Electrostatic Discharge in Semiconductor Devices: An Overview

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Electrostatic discharge (ESD) is an event that sends current through an integrated circuit (IC). This paper reviews the impact of ESD on the IC industry and details the four stages of an ESD event: 1) charge generation, 2) charge transfer, 3) device response, and 4) device failure. Topics reviewed are charge generation mechanisms, models for ESD charge transfer, electrical conduction mechanisms, and device damage mechanisms leading to circuit failure.

Keywords*—*Electrical overstress, electrostatic discharge, empirical models, failure mechanisms, semiconductor devices.

I. INTRODUCTION

Electrostatic discharge (ESD) brings to mind a cold and dry winter day where children shock each other by rubbing their feet on the carpet. The shock felt is an ESD event with significant energy to excite nerve endings, causing pain. The act of rubbing their feet on carpet charges the children's shoes through triboelectric charging and induces a charge on their body [1]. When they touch a conductive object, the charge developed balances, causing a current spike that can be felt. This type of event contains several hundred nanojoules of energy and generates about 3000 V [2]. It can destroy all but the most robust semiconductor devices.

ESD is a subset of the class of failure causes known as electrical overstress (EOS). The EOS class is composed of events that apply conditions outside the designed operating environment of the part. These conditions include voltage, current, and temperature. ESD is defined as a rapid discharge event that transfers a finite amount of charge between two bodies at different potentials. The discharge from a person is modeled as a time-varying current source [3]. The shape of the current is governed by the dynamic impedance between the two bodies. The amount of damage experienced in an integrated circuit (IC) is governed by the current densities and voltage gradients developed during the event.

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ESD damage is the result of an event that occurs at a point in time rather than a gradual chemical process that has an activation energy associated with it. The ESD event is an external influence and is statistical in nature [3]. There is a probability that an ESD event of a selected magnitude will occur during a defined time interval. Development of protection techniques must focus on the external factors that influence generation of an ESD event and on how an IC absorbs the energy in the event. These two items facilitate the development of more robust designs and an environment that presents a lower ESD risk. The IC industry has made large steps toward reducing the ESD environment by educating people handling parts in static-safe practices and providing the equipment to control charge buildup. This is good but by itself cannot provide the complete solution. The second approach is to design more robust circuits. Impediments to this are the design tools needed to model new ESD protection schemes as well as the perception that ESD protection is a lower priority to the design and performance of the circuit. It is inevitable that compromises must be made during the product-development phase. It is critical that ESD robustness be given the same level of importance as circuit performance. The requirement to meet a planned level of ESD must originate at the earliest stage of development. For advanced circuits, special considerations have to be made in the wafer-fabrication process to provide robust circuit elements for ESD protection. The starting point in this case is at process conception to build ESD protection into the process architecture.

ESD improvements follow a twofold approach: 1) produce robust devices through process and circuit improvements and 2) minimize the environmental exposure by providing systems and safeguards to minimize charge generation and charge transfer. This paper provides a detailed review of the ESD event as a foundation of knowledge to recognize improvements in these two approaches. This paper is organized into two major sections: ESD impact and ESD event. The first section discusses the origins of ESD, the types of damage incurred, and the cost associated. The next section describes the ESD event in detail by reviewing the four steps of the event: charge generation, charge transfer, IC response, and device failure.

II. ESD Impact

A. Origins of ESD

ESD events occur because a charge imbalance exists between an IC and another object. Moving parts from place to place during manufacturing and distribution is the main cause for developing this charge imbalance. The second reason is that an IC must come into contact with people and moving machines. As described later in more detail, triboelectrification is the main cause for creating the charge imbalance. This charging process occurs when two dissimilar materials rub together and then separate. People are charged by this method when walking across a carpeted floor or removing a sweater. Machine components charge by this method by rubbing insulative materials during their operation. A single IC is charged by this method, for example, when it slides down an insulative guide rail in a piece of automatic test equipment. All of these methods generate the charge imbalance that allows ESD to take place.

ESD events occur throughout a product's life. ESD first affects the IC early in the wafer-fabrication process. Cleanrooms are good sources for charge-generating materials due to the extensive use of synthetic materials in containers and tools [4]. As an example, the wafer carriers used to transport sets of wafers between tools can charge to well over 20 000 V. This highlights the first problem associated with ESD in a wafer-fabrication facility—particle contamination caused by electrostatic adhesion. The wafers sitting in a charged wafer carrier attract airborne particles, causing them to stick [5]. The bind force of a particle on a wafer is as high as 830 000 psi [6]. One way particle contamination reduces yield is by altering the patterns produced on the circuit. These altered patterns produce shorts or opens, causing the die to be nonfunctional. Additional cleans are required to remove the particles. This adds cost to the wafers, and the extra processing can lower yield.

Another effect in wafer fabrication is the reduction in yield caused by an ESD event. The discharge reduces yield in two ways. First, a discharge to the mask damages the pattern used to define the circuit [4], [7]. An IC is produced by a series of masking steps that define the transistors and interconnects on the die. The masks have the desired pattern defined in chrome. A photolithography operation transfers this image to the wafers. The ESD event erodes the pattern defined on the mask. If the mask is damaged by ESD, then each circuit is printed with this damage. The second mode of ESD damage is a direct discharge to the wafer. This event ruptures oxides and damages junctions [4], [8].

The next stage in a product's life is the assembly operation, where additional ESD hazards are present. The film used during the sawing operation charges to voltages greater than 10 000 V. This film holds the wafer still while it is sawed to separate the die. The die stick to the film. When the die are removed, the film charges. In the assembly operation, the die are handled a great deal. The wafers must be cut to yield individual die. The die are then inspected and placed in packages. Wires are attached to allow signals to travel from the outside pins to the die. Last, the package is formed around the die. All of these operations are capable of producing ESD events [9].

Prior to a product's shipping to a customer and after assembly, some level of additional testing is required. This assures the customer of good product. It could be a simple electrical test at room temperature or a series of burn-in operations and electrical tests over the full temperature range. These are additional opportunities for ESD to occur. The more a part is handled, the higher the probability that an ESD event will occur. The people and equipment used during the testing operation generate the ESD events.

The risk of an ESD event does not stop once the unit leaves the manufacturing plant. In fact, it can increase. The home and office also contain charge-generation sources [10], [11]. The synthetic materials used in carpets, clothes, and seat covers provide sufficient voltage to damage IC's [12]. The cathode-ray tube (CRT) used in computer monitors and television sets is an additional hazard [12]. A large static voltage is generated from all of these sources. A manufacturing plant handles sensitive parts continuously and invests in equipment and procedures to make sure sensitive parts do not become damaged. On the other hand, the customer may not understand the risk and not invest the resources necessary to ensure safe handling of these parts. This is especially true for end users. With the proliferation of the microcomputer, the average person is a computer technician. It is common practice for a person to take the cover off his computer and start replacing components without taking any precautions for ESD. The average person does not consider the hazards of putting memory or a card in a computer. What many people do not realize is that the memory, microprocessor, or adapter board they install can be damaged by ESD. Each of these components comes with warnings that they be handled only at an ESD-protected workstation.

B. Types of Damage

ESD events occur to balance the charge between two objects. The movement of these charges occurs very rapidly, leading to high currents. When the current passes through an object, the impedance of that object establishes a voltage across it. The voltage establishes an electric field in the surrounding objects based on the geometry and dielectric material present in the structure. Both high current densities and high electric fields cause damage on semiconductor devices.

Current-induced damage occurs because joule heating melts a region of the structure. Thin conductive films are the first point of damage. These films are used to connect the circuit elements as well as to act as resistive or inductive components. Thin-film resistors are formed from alloys of nickel and chromium or silicon and chromium. An interconnect is composed of polysilicon, aluminum, or other metals like tungsten, titanium, or molybdenum. Each of these films, except polysilicon, fails by becoming electrically open. The amount of power and energy necessary to cause failure varies by material and geometry

[13]. Polysilicon can become electrically open but also may become lower in resistance [14], [15]. When used as a power dissipation element in an ESD protection circuit, a decrease in resistance allows more energy and voltage to enter the circuit. This may lead to circuit failure [15].

High currents also damage transistors. The emitter-base (E-B) junction of a bipolar transistor is susceptible to these high current spikes caused by ESD. A bipolar transistor may be used as the input to an operational amplifier. In this case, the transistor is made small to minimize input capacitance and leakage. This action also minimizes its capability to handle large current spikes associated with ESD. A leaky or shorted junction results from an ESD event. Bipolar transistors are not the only transistors affected by ESD. The drain of a metal–oxide–semiconductor field-effect transistor (MOSFET) or a diode can also be damaged by an ESD event. The current spike causes the junction to leak more. The mechanism for this is discussed later in this paper.

There are two failure modes associated with high electric fields: dielectric rupture and charge injection. Dielectric rupture is the case where an induced voltage creates an electric field greater than the dielectric strength of the material. The voltage generated may not be high enough to rupture the oxide but the geometry focuses the field at a sharp corner, causing the rupture. When an oxide rupture occurs, a conducting path is established between the anode and cathode. This path is very small. Rupture sites less than 0.1 μm are not uncommon. The energy stored in the capacitor formed by the dielectric is released through this small volume. The result is thermal melting of the plates, causing a conductive filament to form and shorting the plates of the capacitor. The resistance of this short may be hundreds to millions of ohms, depending on the energy absorbed.

The structures that rupture in bipolar circuits are compensation capacitors [13]. These structures have one plate tied to the negative supply pin and the other plate tied to a high impedance node internal to the device. With one plate exposed to the outside world, it is an easy target for ESD damage. Adding elements for protecting this capacitor is difficult because it alters the performance of the circuit. In MOS devices, the gate oxide is the most susceptible to damage [3]. The gate oxide is found in active transistors as well as gated diodes used for ESD protection.

Charge injection occurs because high electric fields at the surface of a junction accelerate the electrons, gaining enough energy to surmount the oxide-silicon energy barrier. Failure analysis does not reveal any physical damage in the oxide. The charge state of the oxide changes. In diodes, the reverse bias I–V characteristic becomes leaky near the breakdown voltage due to the injected charge. This gives the appearance of a shift in breakdown voltage. In a bipolar E-B junction, the charge increases the base current for low collector currents. This decreases the low current gain of the transistor. In MOS devices, a shift in threshold voltage is observed. Charge injection degrades circuit performance but does not cause complete loss of functionality like the previous types of damage.

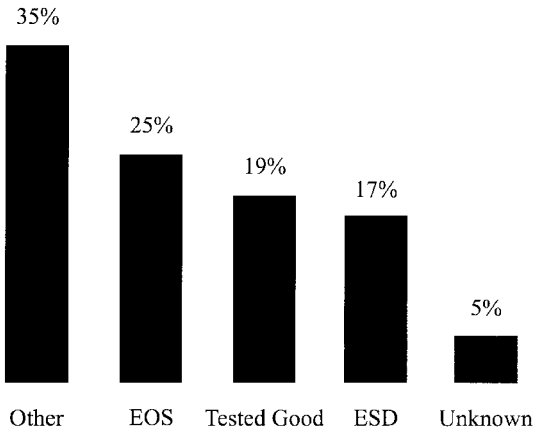

Fig. 1. Field return failure causes.

C. Cost

Fig. 1 shows a pareto chart of the failure causes for all the field returns analyzed; ESD represents a sizable percentage. Wagner *et al.* [16] reported ESD as being the cause of greater than 25% of the failures encountered. These data show a great opportunity for improvement with respect to ESD/EOS related failures.

The cost associated with ESD can be difficult to measure. The tangible costs are material losses, recycle costs, and protection costs. A value can be assigned to each of the factors. The more difficult costs to measure are the intangible costs related to delays and the loss of customer confidence caused by failed product. Each of these is covered in this section.

Material losses are the easiest to identify because these are the costs associated with the parts that have failed. The costs include raw materials and the value added during the manufacturing operations prior to the part's failing. This cost also includes the analysis effort and support cost associated with identifying the cause of ESD and fixing the source of the ESD event. For many cases, the number of failures does not justify the cost of identifying the cause, so the ESD source is not corrected and a steady but small stream of failures occurs. In some cases, an excessive number of failures (typically greater than 20%) occurs; then the entire group of parts must be scrapped from production. This condition is very expensive. If rescreening is allowed, then the material may be rescreened and recycled through some or all of the manufacturing operations. The rescreening may be a simple electrical test or may require testing and burn-in. It is important that the source of the ESD be corrected so that additional failures do not occur during the recycle attempt.

The cost associated with recycling includes not only the labor and equipment costs but also the costs associated with a schedule slip, decreases in capacity, and the opportunity cost of not running other material. The cost of labor and equipment is a direct cost of the salaries, overhead, and equipment depreciation. These are well-documented numbers and should be available within a company. They are used to determine the price of a device. It is more

difficult to calculate the cost associated with a schedule slip unless the contract has penalties for being late or rewards for early delivery. The decrease in capacity comes from having to process each part multiple times. For example, if every ninth lot has to be recycled, it gives the effect of a 10% reduction in capacity because only nine lots of product are shippable for every ten lots processed.

The cost of protecting sensitive devices is a cost shared by all products. Each product benefits from these measures. This cost includes the protective equipment used in production (ionizers, monitors, smocks, etc.), packaging and transport materials, training and administrative systems, and development systems. These items insure that an ESD-safe environment is provided and that research and development into improved ESD designs is funded.

The intangible costs come from all the "explaining" a vendor must provide to a customer when ESD failures occur. A loss in customer confidence occurs. Schedule slips as well as a perception of low quality from all of the failures may strain the relationship a customer has with his vendor. This leads him to look for other vendors for similar parts and to only buy his original vendor's parts when there are no other alternatives. The second part of the intangible costs is the opportunity cost associated with a failed device. When failures occur, the support personnel must determine the cause of the failure and a corrective action to prevent its occurrence. If this is not done and is instead ignored, then there is a chance that it will occur again. Their time could be more productive if they were doing the work necessary to get new products in place.

III. ESD Event

This section is divided into four topics based on the steps involved during an ESD event. There are four major steps. The event starts by a charge-generation mechanism's creating an imbalance of electrons between two bodies. The second stage is the actual ESD event, where the charge is transferred. The three models for charge transfer are reviewed. These are the human body model (HBM), machine model (MM), and charged device model (CDM). The third stage reviews the IC's response to the inrush of charge. Equivalent circuit models at the package and die level are reviewed along with the charge-conduction mechanisms in the IC. These items define the current and voltage levels induced in the circuit. The current and voltage levels determine the power delivered to the circuit. The capability of the IC to absorb this energy leads to the last stage—survival or failure. The last section reviews the damage mechanisms associated with ESD. The topic of latency is also defined and discussed in this section.

A. Charge Generation

The charge level reached in any generation mechanism is dependent on three items: generation process, material characteristics, and dissipation sources. Each of these factors is reviewed. There are three major charge-generation processes. These are triboelectrification, induction, and conduction. The first process is the most common in a manufacturing or laboratory environment. Triboelectrification requires physical contact between two different materials. An example is shown in Fig. 2. During the time these materials are in contact, an exchange of free electrons takes place based primarily on the materials' respective work functions. When they are separated, the free electrons redistribute and balance if both materials are conductors, but if one or both are insulators, a residual charge is left in the insulator. This excess charge generates the voltage differential. The measured voltage is based on the capacitance of the system. The act of rubbing the materials together increases the charge concentrations. The amount of charge generated depends on the contact area, pressure, and friction between the two materials [17]. The polarity of the charge depends on the materials and is predicted from the work-function differences between the materials [17]. Triboelectrification is enhanced by a smooth surface, large contact area, high applied pressure, and high rubbing speed [12].

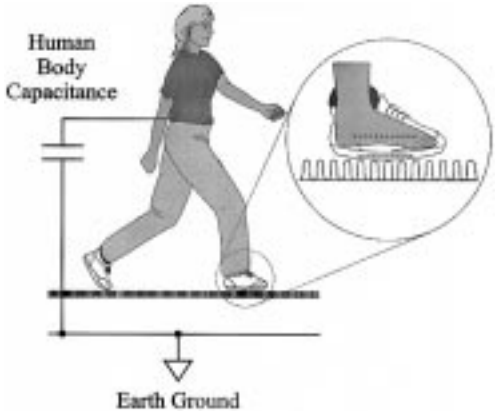

Fig. 2. Triboelectrification illustration.

An example of triboelectrification was given at the beginning of this paper. When a person walks across the carpet, they become charged by the process of triboelectrification. The type of footwear and carpet play an important part in the charge levels generated [18]. Leather shoes are the safest by generating the smallest charge and having a high capacitance [18]. The higher capacitance keeps the voltage level lower. The polarity of charge depends both on the type of sole and on the finish applied to the floor. All nongrounded surfaces can triboelectrically charge [7]. Once charged, this surface can source a field that causes the next type of charging—inductive charging.

Inductive charging is a two-step process. It is illustrated in Fig. 3. A conductive object "B" comes into close proximity with a charged object "A." Part of the field terminates on "B," resulting in an internal separation of charge. Momentarily grounding "B" removes the polarized charge. When "A" is removed from the area, a net charge exist on "B" but opposite in polarity from what existed on "A." Grounding "B" once again balances the charge. This type of event can have two current pulses. One occurs while the charged object is close and the other while it is away.

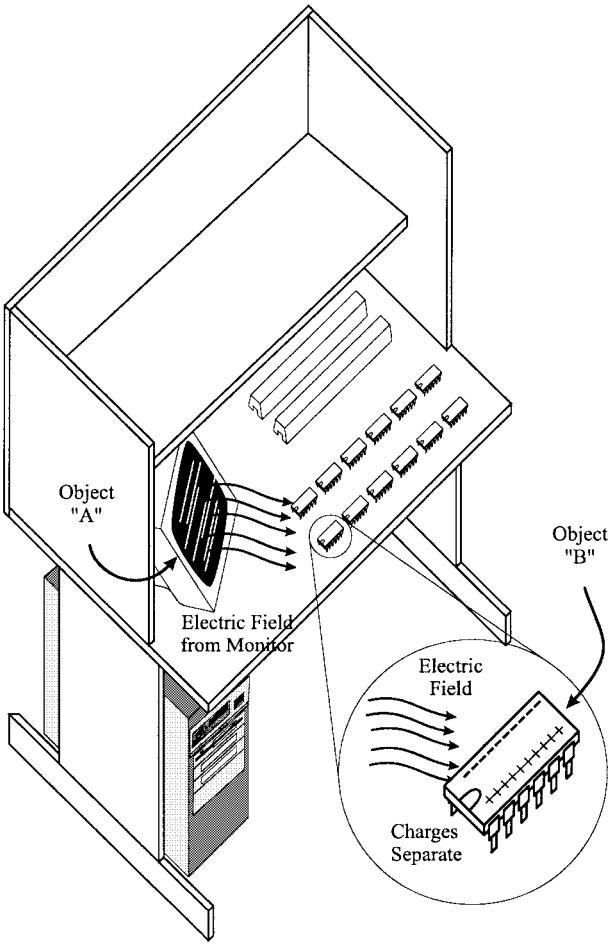

Fig. 3. Induction illustration.

The current is limited by the impedance in the grounding path, which can be very small. The event can generate very high current pulses. The transient caused by induction is similar to a CDM event [7]. The magnitude of the energy in this transient depends on the strength of the field and the device coupling to that field [7].

The use of computers in the work environment provides a strong source for inductive charging. Paperless manufacturing puts computers at each stage of a part's journey. The journey starts where the raw materials are logged into the inventory control system and finishes with printing the shipper to send the parts to the customer. The CRT in the computer monitor has a high potential on its surface and can induce a charge on other objects that come into close proximity to it [12]. When an IC is handled around a computer monitor, the monitor induces a charge imbalance in the part. If the part is picked up with metal tweezers or comes into contact with any other charge sink, ESD damage can occur [1]. It is a wise practice that sensitive components be handled in an area free from charged surfaces like monitors and insulative materials like cups and paper. These items should be kept away from the work area.

The last process to discuss is the most straightforward charging method. Conductive charging involves the physical contact and balancing of voltage between two systems

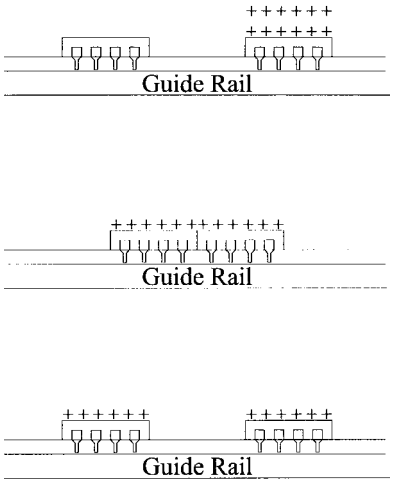

Fig. 4. Conduction illustration.

or objects at different potentials. This is illustrated in Fig. 4. A charged object is brought into physical contact with an isolated object of lower potential. During the time of contact, charge is transferred to the lower biased object until the potentials balance. When the objects are separated, body A has accumulated a charge of the same polarity as body B. The voltages will be equal and the charges on each will be related by the capacitance of each body. The total charge in the system of two objects remains constant.

An example of conductive charging is found during automated testing. A handler moves the parts from the trays or tubes and presents them to the test system for electrical testing. In this process, they continuously contact each other. If one part becomes charged by triboelectrification, it transfers part of its charge by conduction to an adjacent part. The charging event damages both the sourcing and sinking part. The impedance is very low between the parts, so high currents are generated for relatively small amounts of charge. The capacitance of a part is small, so high voltage levels are achieved with small amounts of charge.

The types of materials used around sensitive electronic components are important in controlling the ESD threat. Insulators are especially bad because they readily charge by triboelectrification and can source the electric field for inductive charging. In a static-safe work area, plastic bags, purses, paper, styrofoam, and similar materials must be avoided. A safe work area will be devoid of these materials. If insulators are bad, then are conductors good? This may seem correct but it is not. Conductors have two major problems. First, conductive surfaces pose a shock hazard to people working around them. If an electrical fault in a piece of equipment occurs, it would transfer the energy to the table's surface, shocking the person. The second problem is that the conductive surface acts as a large charge sink or "virtual ground." A metallic surface absorbs large amounts of charge without raising its potential significantly. This presents a low impedance discharge path for the parts. Very fast discharge pulses with high current magnitudes result. These high current levels damage IC's.

The best material to use around sensitive IC's is a static dissipative material. This class of material has a resistivity range in the order of 10^5 to 10^9 Ω per square. This material should be used for work surfaces, tools, and in handling equipment. Last, the parts themselves should be stored in static dissipative containers. Static dissipative material provides a path for the charge to bleed off in a controlled manner so that high current spikes are avoided and low voltage levels are maintained.

An example of using static dissipative material instead of insulative material is described by Bernier and Hesher in [19]. With the growth of semiconductors has come the increased use of automatic handlers during electrical testing operations. This equipment eliminates the expensive and time-consuming operation of hand testing each part. This is good from the ESD standpoint because it removes the human as the source of ESD damage. It nonetheless introduces another problem. Some handlers have parts that are made from insulating materials. These insulating parts exist in the guide paths and at the interface to the temperature chamber. As a unit slides down the nonconductive guides, it charges by triboelectrification or induction. Once the charged part comes into contact with the test socket, an ESD event occurs, damaging the unit. A way to minimize these effects is to machine the insulated parts out of a static dissipative plastic instead of a highly insulative material. This minimizes any buildup of charge in the machine.

The work environment where the parts are handled also is important. One of the most important parameters for a work area is the relative humidity. The amount of moisture in the air controls air resistance. At higher levels of humidity, it is more difficult to generate and sustain a charge. This fact is most noticeable in the winter, when heaters dry the air, making it easier to be shocked after walking over a carpet. Low relative humidity means 20 to 30 times higher voltages generated for the same set of conditions [20]. Walking across a carpet can generate 35 kV in low humidity compared to 1.5 kV in high humidity [20]. Relative humidity is typically controlled to between 30 and 70%. The low limit is for static control. The high limit is governed by other equipment factors, such as calibration controls.

Relative humidity is a naturally occurring atmospheric control for charge generation and elimination. There are also many artificial environmental controls that have similar effects. A typical static-safe work area is illustrated in Fig. 5. Many of the static-control techniques are illustrated. Local and room ionizers control static by placing a balanced number of ions in the air, increasing its conductivity. This acts to dissipate any charges that build up on objects. The use of lab smocks, dissipative floors, and shoes with ground straps aids in controlling the charges on people handling parts. It does so by allowing a path for any charge to bleed off in a controlled manner. Work surfaces and equipment are also grounded to preclude charge generation. Proper installation and use of this equipment is necessary to prevent harm to the people in contact with the ESD protection equipment.

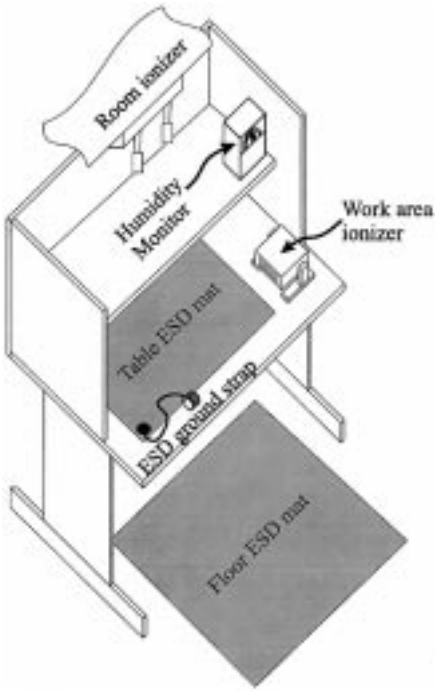

Fig. 5. ESD controls used in an electronics laboratory.

B. Charge Transfer

An ESD event can be modeled as a two-body system. Body "A" could be an operator at a test station and body "B" could be the next part for test. As described earlier, a charge imbalance develops between these two bodies by one of the three generation mechanisms described. The charge imbalance also translates into a voltage imbalance based on the capacitance of each body. When the operator picks up the part for testing, the two bodies come into contact with each other. Charge transfers from the higher potential body to the lower potential body until the voltages between them are equal. At this point, the ESD event is over. The characteristics that define the current during the event are the capacitance of the two bodies and the impedance between them during the event. It is these two parameters (capacitance and impedance) that differ in the three models for the transfer process.

The IC industry has standardized on three basic models to define how charge is transferred during an ESD event. The models are based on the element holding the charge and the discharge impedance. They are the HBM, MM, and CDM. Each of these has standards or proposed standards defining the equivalent circuit model and how testing and calibration are to be done. These models intend to simulate reality but do not cover all possible variables that influence a real ESD event. As such, they should be used only to compare robustness of different design schemes and not as an absolute measure of a design's ESD capability [3], [21]. This section reviews each of these models in detail.

The HBM is the most popular ESD model and the one most people use to compare ESD threshold levels between parts [22]. As the name implies, it is designed to model the ESD event coming from a person's touching

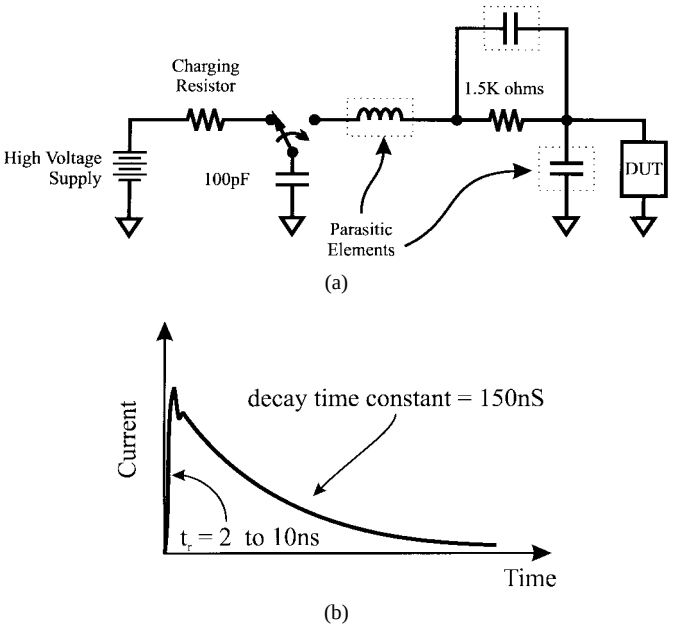

Fig. 6. HBM ESD with parasitics. (a) Schematic. (b) Current waveform.

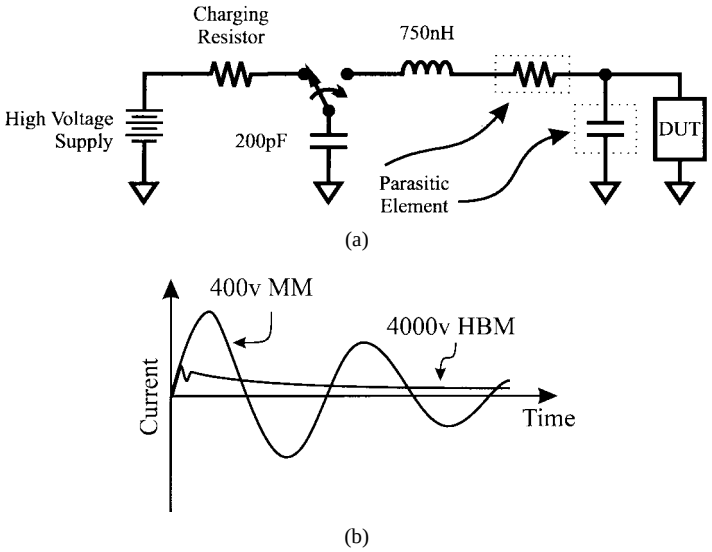

Fig. 7. MM ESD with parasitics. (a) Schematic. (b) Current waveform.

an IC. The model assumes that a person is standing upright [23].[1] Fig. 6 illustrates both the HBM schematic and the current waveform assuming zero device under test (DUT) impedance. The differences seen between testers are due to the parasitic impedance shown in Fig. 6 [22], [26]. Because of the large series resistance in the HBM, this ESD event can be modeled as a current source with the current waveform shown in Fig. 6 [3], [24]. The energy content in an HBM event follows the energy stored in a capacitor (i.e., 1/2 C-V^2). At 4000 V, a total charge of 0.4 μC and 800 μJ of energy is available, but only a small fraction of this is absorbed by the IC [24]. For the HBM, most of that energy is dissipated in the source resistance. The critical parameters in the HBM are series inductance, stray capacitance, and series resistance.

In real-world situations, a person will have a resistance and capacitance that differs from this model. The charge accumulates in the shoes and induces a charge on the body [1], [25]. Chase and Unger [18] showed capacitance from 167 to 514 pF depending on the type of footwear worn. The thickness and material type of the sole determine the capacitance and triboelectrification characteristics. A person's skin resistance also varies depending on the levels of oiliness and the amount of perspiration on the skin. The resistance can vary from 1000 to 100 000 Ω. If a metal object is held in the hand while touching the DUT, the resistance is lowered, causing faster rise times and higher peak currents [20].

The MM (shown in Fig. 7) is similar to the HBM, with the substitution of a 0.75-μH inductor for the 1500-Ω resistor, increasing the capacitance to 200 pF [26]. This model is intended to represent the type of damage caused by equipment used in manufacturing. It represents a worst case HBM event and produces damage similar to the HBM but at much lower threshold levels.[2] The inductance value in the model is the most critical parameter because it controls the rise time of the current during the discharge.

The CDM is the newest model and also the most difficult to reproduce [22].[3] It is very sensitive to parasitics in the test hardware. This model is intended to simulate the event that occurs from a charged packaged part's subsequently discharging into a low impedance ground. This ground can be a hard grounded surface or a large charge sink like a metal work table or tool. This could occur during testing where a part is triboelectrically charged in a handler. When the part comes into contact with the tester's pins, it discharges. The discharge impedance in real life is close to zero, but it is finite and small in an ESD tester. This is where the variability between testers comes into play. An illustration of this type of event is shown in Fig. 8. The peak currents are much higher than in the HBM and the rise times as well as the duration is much shorter. The rise time is limited by the inductance and resistance in the current path. For many packages, this is the bond wire impedance of $\sim$0.5 nH.

There are two methods for CDM ESD testing that depend on how the part is held during the ESD testing. They are referred to as socketed and nonsocketed [27]. The test setup shown in Fig. 8 is for the nonsocketed method. The socket version produces more severe damage and in some cases a different failure mode than the nonsocket version [27]. Further references to CDM ESD in this paper refer to the nonsocketed type of events.

A CDM event occurs so rapidly that the protection circuits may not turn on in time to clamp the voltage to

[1] This model is defined in *Revised Electrostatic Discharge Sensitivity Testing—Human Body Model*, ESD Standard S5.1-1993. A revised specification is expected this year.

[2] *Electrostatic Discharge Sensitivity Testing—Machine Model*, ESD Standard S5.2-1994.

[3] One draft standard is found in *Electrostatic Discharge Sensitivity Testing—Charged Device Model*, ESD Standard DS5.3, 1996.

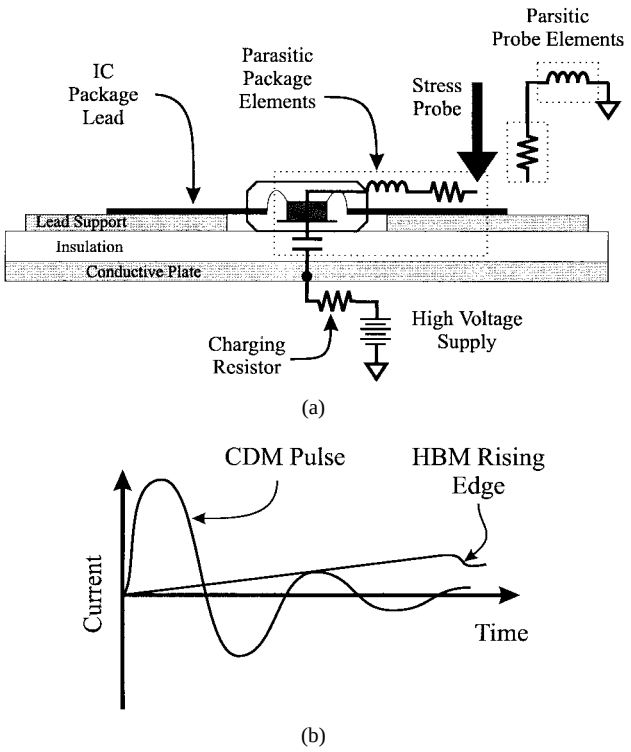

Fig. 8. CDM ESD with parasitics. (a) Schematic. (b) Current waveform.

an acceptable level [3]. This can result in an oxide rupture to the protection circuit or the circuit being protected. An ESD pulse on the drain of an n-channel (N)MOS device causes the drain to enter avalanche breakdown. A portion of the avalanching electrons have sufficient energy to be injected into the oxide. The injection point is very small. This focused charge injection allows the gate dielectric to ionize rapidly [21]. Once a conductive path is established through the gate, the energy stored in the gate capacitance is discharged through this small path, destroying the oxide.

In the CDM event, the charge storage location is in the device itself rather than an external object. The package has many capacitors for charge storage. These include the capacitance between the conductive layers of the package and the gate and junction capacitance on the die, as well as the interconnect capacitance on the die. The major charge storage element is the isolation technology of the die substrate and die attach paddle [28]. This storage element is discussed in the next section. CDM threshold levels improve if this capacitance is discharged through a correctly sized element. Package size and design strongly influence the CDM threshold levels of a device [29].

C. IC Response

The above discussion shows how a charge imbalance is developed and the three configurations used to model the transfer of charge. The next phase of an ESD event is how a circuit responds to this pulse of charge. Once an ESD event is initiated, charge begins to redistribute. This movement of charge generates currents and induces voltages. An ESD event is simply a redistribution of charge and therefore a charge-driven mechanism. The rate at which charge moves defines the currents, and the capacitance of the structure they move into defines the final voltage. The voltage developed also has a transient component defined by the product of the current and the impedance of the conducting path. How a device withstands these currents and voltages determines if it continues to operate correctly. This section reviews the discharge paths taken through a typical IC. One challenge in design is understanding the various current paths (both parasitic and designed) and their thermal and electrical characteristics.

The starting point for understanding the response to ESD is to look at the construction of a typical IC as shown in Fig. 9. The die is placed in a package and connected to the outside world through bondwires and the interconnect of the package. It is through these pins that the ESD event passes. The charge from an ESD pulse first travels through the package interconnect and then to the die. The package interconnect acts as additional impedance between the ESD source and the die. The higher the impedance, the more protection is given to the circuit. Higher resistance dissipates more of the energy from the ESD pulse prior to its reaching the die. Higher inductance slows the rise of the current pulse. These are desired effects on the ESD pulse, but unfortunately, they also affect the incoming electrical signals in the same way. In high-performance packages, impedance is minimized to get the best performance from the circuit. The package equivalent circuit as seen by an ESD event is shown in Fig. 10. The charge storage in the package is between the different conducting planes. The largest plane is in the die attach to the die's surface. Here, the charge is stored in the isolation technique (junction isolation, dielectric isolation, or silicon on insulator) used by the circuit to separate each transistor. Minimizing this die-level capacitance reduces the quantity of charge stored and raises the CDM tolerance. This can be seen by higher CDM thresholds for small packages versus larger packages in the same technology.

The next point in the charge's path is the die. The active part of the IC is contained in a thin layer at the top of the silicon die, as shown in Fig. 9. This thin region has conductive layers connecting each circuit element to form the circuit function. As the charge moves through the die, it sees both passive and active elements. An equivalent circuit schematic for the die is shown in Fig. 11. This figure shows a simple ESD protection network. In the case of an unprotected input, the diodes and resistor would be removed, leaving an exposed gate oxide to absorb the ESD event. The threshold would be very low in this case. The ESD charge passes through both the circuit elements used to implement its function and the parasitic elements that are present but not active in normal circuit operation. The parasitic elements are enabled when a set of voltage or current conditions is established by the conduction path. These parasitic elements can account for the odd behavior observed during ESD testing. Some devices consistently fail at 500-V HBM ESD, but the same design consistently passes 1000 V. This unexplained result occurs because

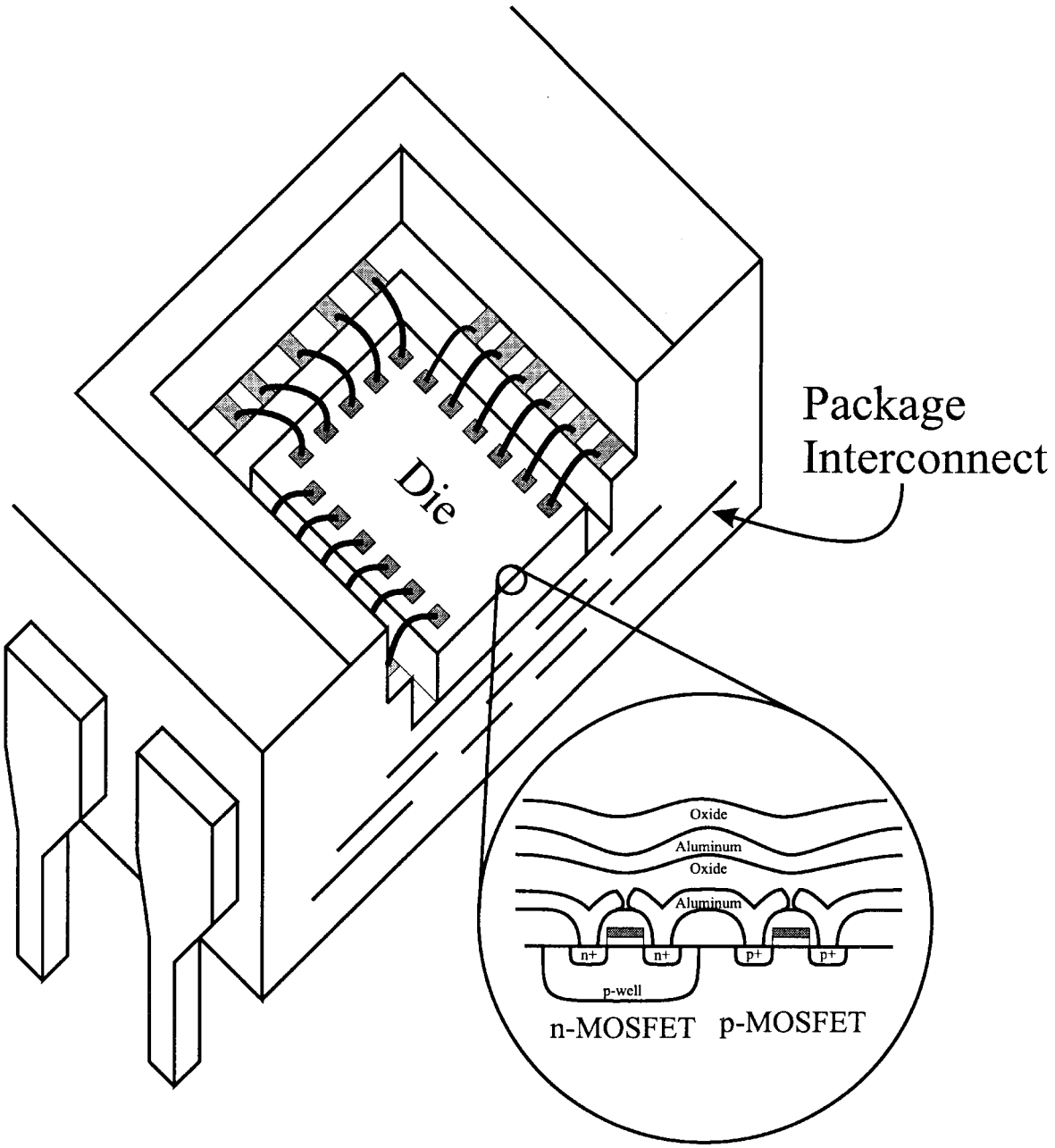

Fig. 9. Typical IC package.

different conduction paths are active, generating different internal voltages and power dissipation based on the level of the ESD event.

Examples of some parasitic devices are also shown in Fig. 11. One is the parasitic bipolar transistor in the NMOSFET. This device helps dissipate charge by entering snap-back during breakdown. The terminal voltage is reduced once snap-back is entered, thereby lowering the power dissipated. The illustrated protection concept is similar for all protection schemes: allow a low impedance discharge path around the circuit element you wish to protect. The difficulty is designing an effective ESD protection circuit that does not interfere with normal device operation. For HBM and MM ESD, the charge enters the IC through one pin and exits through another. Pins are stressed in pairs. During ESD testing, each pin-pair combination is stressed with both positive and negative current. In a CDM event, the charge resides in the circuit, so the discharge is through only one pin at a time [30]. For adequate protection, all combinations of pins must be protected [31].

The conduction path taken through a circuit is difficult to predict because the magnitude of the current pulse defines which path or paths conduct the charge. Fig. 11 shows three possible current paths for an HBM ESD event. Path "A" assumes that a positively charged person contacts an input pin. The return path is assumed to be the positive supply pin V_{DD}. For this case, the input protection diode is in forward conduction. The voltage drop across the diode is low, as is the power dissipation. The volume in which the power is dissipated is high and is almost the entire

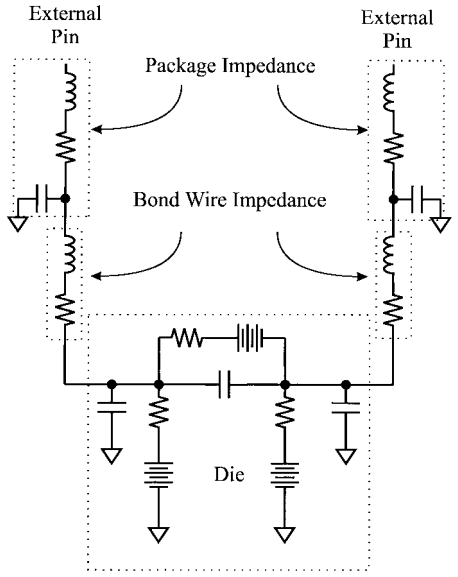

Fig. 10. Package equivalent circuit as seen by an ESD event.

volume of the diode. The power is dissipated over a region, extending away from the metallurgical junction toward the anode and cathode contacts. This translates to a low power density for the device. The diode is in its most robust conduction mode. If the conduction path were changed to the ground pin instead of the supply pin, the diode would be in its worst conduction mode. For this case, the diode is in reverse-bias avalanche breakdown. The breakdown voltage is much higher than the forward voltage, so the power dissipated in the element is very high. Most of this voltage is dropped across the narrow depletion region located around the metallurgical junction. This translates into a small dissipation volume and a high power density. A much larger diode is needed to absorb the energy in an ESD event that causes a reverse breakdown conduction mode.

Another mode of conduction often overlooked is the capacitive coupling of an event to an internal element. This is shown in Fig. 11 as conduction mode "C." An ESD pulse applied to V_{DD} causes the voltage on V_{DD} to change rapidly. The gate capacitance of a large p-channel MOSFET transfers the rapid dv/dt signal to an internal logic node. The resulting current, $I = C\,dv/dt$, causes the smaller circled transistor to be destroyed. Destruction comes from high current densities' shorting the transistor from drain to source.

The above discussion illustrates three conduction mechanisms that occur in an IC during an ESD event. The linear conduction mechanisms are easily understood and will not be discussed here. These are $V = IR, I = C\,dv/dt$ and $v = L\,di/dt$. The focus in this paper is on the nonlinear conduction mechanisms summarized in Table 1. Each one is illustrated with its typical I–V characteristic in Fig. 12. Each conduction mechanism has an upper limit on the amount of current that is allowed without destruction. Charge injection and dielectric breakdown are the two mechanisms that cause physical changes to the dielectric layer that are difficult if not impossible to anneal out. If one of these mechanisms is active, a damaged device results. Forward conduction and silicon controlled rectifier (SCR) action are the two best conduction mechanisms by generating the lowest power and spreading it over the largest volume. Snap-back is next, with junction breakdown being the worst, as described earlier. There are tradeoffs with each protection technique. With SCR protection, the risk of latch-up increases.

Rarely does one find a perfect device or circuit. A lot of electrical testing is necessary to remove the defective population from the shippable product. Imperfections in the design or construction of an IC also reduce the ESD threshold. It is more difficult to detect these imperfections with simple electrical tests because they may only be active at the extreme stress conditions imposed by an ESD event. These imperfections act as concentrators for the energy or electric field during an ESD event. The imperfections apply to both processing defects (crystal faults and oxide pinholes) and design nonuniformities. The imperfections make the design more sensitive by focusing the destructive energy toward a specific point instead of uniformly over the entire region.

Two types of geometry or design imperfections from an ESD viewpoint are illustrated in Figs. 13 and 14. Fig. 13(a) shows a device layout that causes a nonsymmetric current density along its width [32]. The resistance in the drain and source regions reduces the bias in the remaining width, causing the transistor to conduct most of the current on one end. This type of layout results in damage close to the entering metal. It is important that the entire width conduct uniformly so that no single spot carries all the current [33]–[35]. A drain-to-source short results from this stress condition. Fig. 13(b) is a better layout. It allows symmetric current flow. Fig. 14(a) shows a silicon on sapphire (SOS) transistor cross sectioned along the channel width. The points at each end of the transistor where the polysilicon steps down the side of the mesa are high field regions. A voltage transient caused by an ESD pulse can rupture the oxide at these points before the normal gate is damaged. Transistors exposed to ESD voltage transients should incorporate a circular design, shown in Fig. 14(b). This design removes the high field points and produces a more robust structure against ESD damage.

Processing defects can severely affect the ESD performance of device structures. Fig. 15 shows an emission microscope (EMMI) image of a transistor as the drain voltage approaches breakdown. The EMMI is a tool to detect low levels of light that accompany five electrical phenomena: 1) avalanche luminescence, 2) dielectric luminescence, 3) forward bias emission, 4) thermal radiation, and 5) saturated luminescence. The light emitted shows that the junction is in breakdown at this point. A crystal defect exists here and reduces the local breakdown voltage at this point. As a result, this spot absorbs most if not all of the energy during a transient. Fig. 16 shows the damage after an EOS event. Clearly, this defect site lowered the tolerance of this structure.

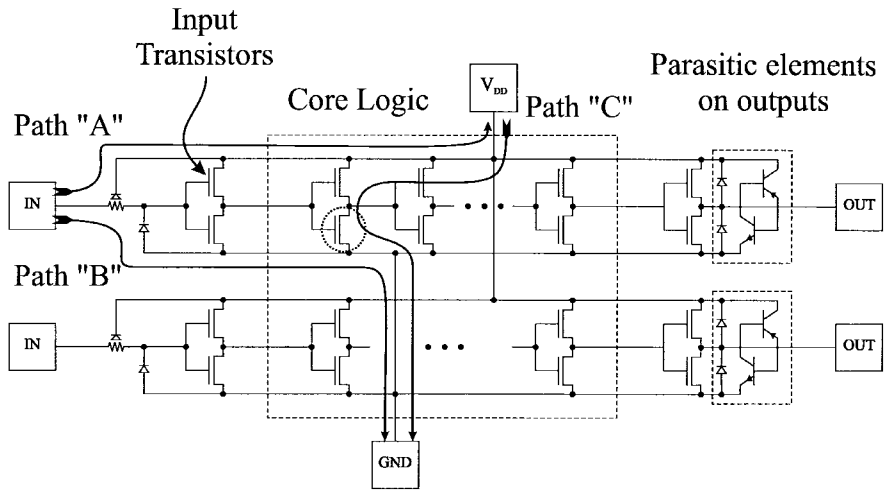

Fig. 11. Digital circuit schematic as seen by an ESD event.

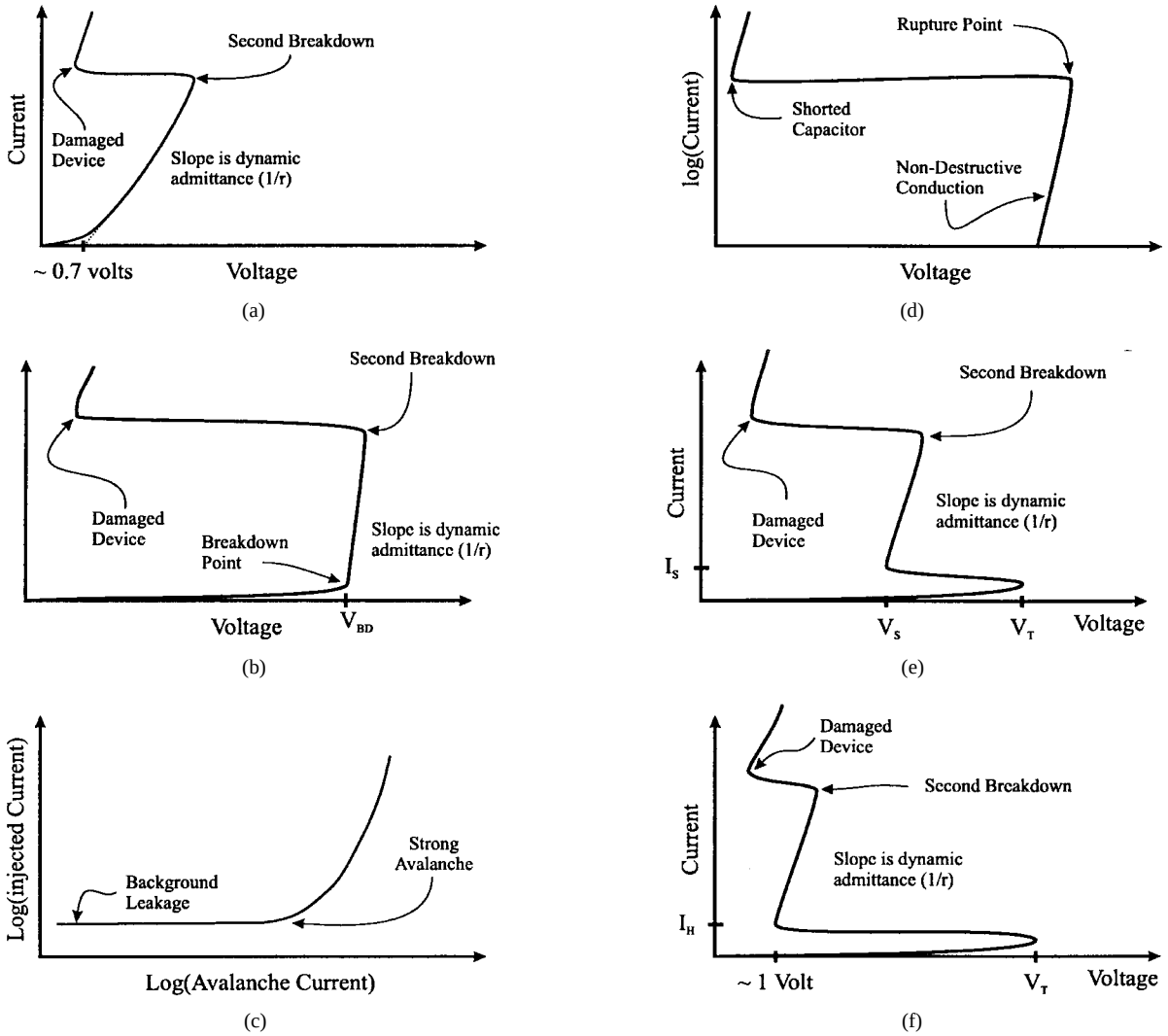

Fig. 12. Nonlinear conduction mechanisms' I–V characteristics. (a) Forward conduction. (b) Junction breakdown. (c) Charge injection. (d) Dielectric breakdown. (e) Snap-back. (f) SCR.

It is difficult, if not impossible, to design around processing defects. Testing is also not a viable option because of the random nature with which defects occur and the stress conditions necessary to detect them. The only effective method is to reduce their numbers by continuous improvement of the wafer-fabrication process. This is accomplished by designed experiments and specially designed test structures and test techniques that are capable of detecting the defects

Table 1 Nonlinear Conduction Processes in an IC During an ESD Event

Conduction Process	Description
Forward Conduction	• Power dissipated over entire device region. • Parasitic resistance controls power dissipation. • Total power dissipation is low to medium. • Full recovery possible.
Junction Breakdown	• Power dissipated in depletion region. • High power dissipation. • High power density (small volume). • Parasitic resistance controls current capability. • Full recovery possible.
Junction Avalanche Dielectric Charge Injection	• Electric field at surface controls injection. • Oxide charge generated by current flow. • Physical change in microstructure of oxide.
Dielectric Breakdown	• Electric field causes current flow in oxide. • Field intensity exceeds dielectric strength causing a short. • Energy stored in capacitor discharged into small site causing rupture. • Physical change in microstructure of oxide.
Snapback	• Bias voltage exceeds trigger voltage, V_T. • Terminal voltage decreases to sustaining voltage, V_S. • Lowering voltage reduces power dissipation. • Parasitic resistance controls terminal voltage and power dissipation. • Full recovery possible.
Silicon Controlled Rectifier (SCR)	• Conduction triggered by displacement or avalanche current. • Terminal voltage very low. • Good protection device. • Full recovery possible.

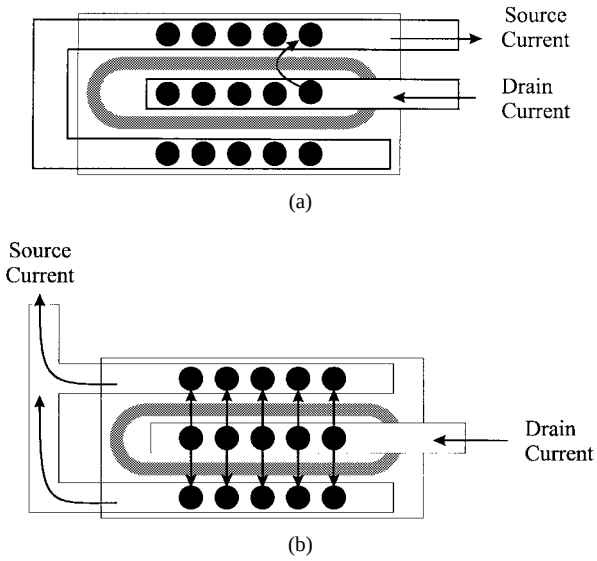

Fig. 13. Induction illustration.

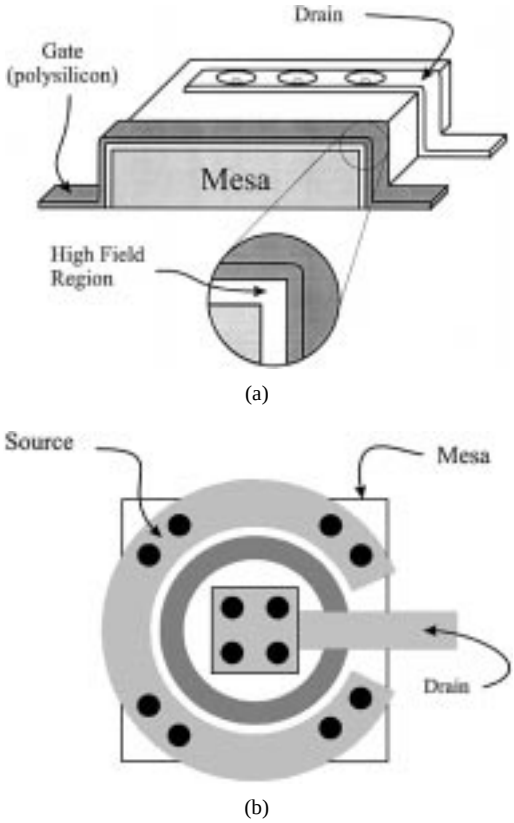

Fig. 14. Electric field optimization for ESD protection element. (a) Poor design. (b) Good design.

of importance. A complete treatment of defect density reduction is not the subject of this paper. The reader is referred to books and journals on statistical process control, design of experiments, defect density reduction, and test structure design for more complete treatment of this subject.

In the case above, improvements in wafer processing are required to reduce the defect density, but some advances in wafer processing also lower the ESD tolerance. Two examples are silicided junctions and lightly doped drain (LDD) structures, as shown in Fig. 17. Silicided junctions reduce contact resistance and LDD structures minimize the effects of hot electron degradation. The use of silicides on output devices can decrease the ESD threshold by 50% [36]. Both LDD's and silicides reduce the ESD

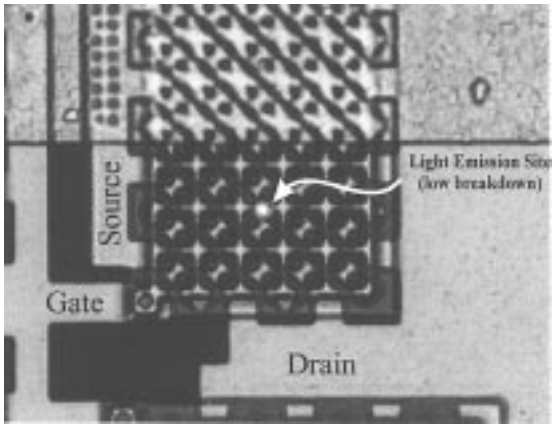

Fig. 15. EMMI photograph showing defect site causing lower breakdown of junction.

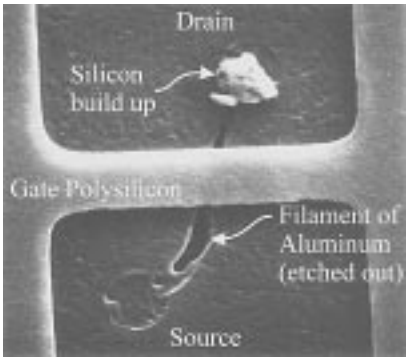

Fig. 16. Resulting short site when the transistor was subjected to EOS.

threshold of devices [32], [33], [36]. The silicide material is a low resistance layer on top of the normal drain and source diffusion. Because the relative resistance of silicon to silicide is high, most of the current is carried in the very thin silicide region. The low resistance of the silicide also reduces the natural balancing of the current across the width of the transistor. With silicide present, all the current may flow in a small fraction of the total transistor. This causes the current density to increase, producing damage easier. LDD structures have a similar effect by increasing the resistance through a transistor and also changing the conduction characteristics in the transistor during the ESD event. These changes produce higher power dissipation, resulting in damage to the transistor at lower threshold levels. Both of these advanced techniques should be carefully applied in elements designed to absorb ESD transients. These two examples show that all aspects of a process must be reviewed against how it effects the ESD capability of a finished product.

D. The Aftermath

Once an ESD event is over, the task of assessing a failure begins. This is the last stage of an ESD event. The question to answer is, "Did the part survive?" A clear definition of the failure is required to assess this. The electrical test specification defines the point of failure.

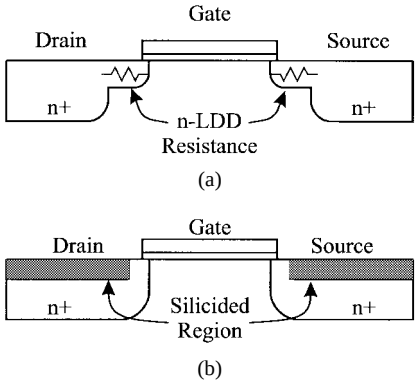

Fig. 17. Advanced process techniques that degrade ESD tolerance. (a) LDD structure. (b) Silicided junction.

Table 2 ESD Classification from EOS/ESD Standard S5.1-1993

Classes	Voltage Range
Class 0	0 - 249 volts
Class 1A	250 - 499 volts
Class 1B	500 - 999 volts
Class 1C	1000 - 1999 volts
Class 2	2000 - 3999 volts
Class 3A	4000 - 7999 volts
Class 3B	≥ 8000 volts

It defines the leakage, drive current, timing tests, and functional tests that must be successfully completed to be considered good. A limit on the amount a parameter is allowed to change may be needed. This is considered a delta limit. When making comparisons between different parts or technologies, it is important to know the test criteria used and the ESD tester specification [37]–[39]. This ensures that the results can be compared. It would be incorrect to compare the ESD threshold of a low-noise precision amplifier to a microprocessor. The amplifier has tight limits on bias current, and small changes in leakage current cause it to fail. The same level of change in the microprocessor would not be of concern. There are three types of failure modes: 1) hard failure—physical destruction or damage, 2) soft failure—temporary change in logic function (i.e., flip-flop changed state), and 3) latent failure [1]. The first of these is addressed in this section. The last will be addressed in a later section. Soft failures are not addressed in this paper because they occur during powered-on operation, which is not the focus of this paper.

All of the failure classifications in use base their levels on the maximum voltage applied without failure. This voltage is the open circuit voltage of the charged capacitor in the previous discharge models. The classifications are used as a guide to people handling parts. The lower the rating, the more sensitive the part is to ESD and the more precautions are required to keep them safe. The classification standard used in the governing procurement document or industry standard is the appropriate one to use in classifying parts. Table 2 lists the classification standard for ESD Standard S5.1-1993. A "Class 0" part is the most sensitive and requires extra precautions beyond what is normally used in manufacturing. These precautions can include dedicated

Table 3 Damage Mechanisms Caused by an ESD Event

Damage Mechanism	Description	References
Filamentation	**Cause:** Current flows in localized regions crating a melt filament. Redistribution of dopant atoms and crystal damage causes high field and leakage currents. Shorted junction occurs in worst case condition. **Correction:** Reduce defect densities. Insure uniform current flow across junction.	[64 ,65 , 66, 67]
Charge Injection	**Cause:** Avalanche breakdown of junction injects hot carriers into oxide. Shift in surface threshold affects V_T in MOSFET, h_{fe} in BJT and breakdown voltage in diodes. **Correction:** Minimize electric fields at junction surface.	[51, 68, 69, 70, 71, 72, 73]
Oxide Rupture	**Cause:** ESD current induce voltages. Developed electric fields exceed dielectric strength resulting in a rupture of the dielectric. **Correction:** Minimize sharp corners to lower field intensities. Reduce defects densities.	[74, 75, 76, 77, 78, 79, 80]
Thin Film Burn-out	**Cause:** Power density in the film exceeds its capability. Joule heating causes film to melt resulting in fusing. **Correction:** Increase cross sectional area. Use film with higher melting temperature.	[14, 15, 43, 44, 45, 46, 47, 48, 49, 81, 82, 83, 84, 85]
Contact Spiking	**Cause:** Failure mode is similar to filamentation. After second breakdown a melt filament intersects an aluminum contact. An interchange of aluminum and silicon takes place shorting the junction. **Correction:** Space contacts away from the junction. Insure uniform current flow across the junction.	[33, 42, 86]

people, special work areas, and packaging materials. These precautions would be used for all parts, but the cost involved reserves their use for only the parts that require it.

Circuit-level failures manifest themselves as a change in a measurable parameter. Examples are input leakage, supply current, bias current, and offset voltage. In extreme cases, the total loss of functionality occurs. The circuit design and function dictate the sensitive parameters. For op-amps, the sensitive parameters are offset current, offset voltage, open loop gain, and common mode rejection ratio. The compensation capacitors and input stage are the weak links in the design. When a compensation capacitor fails, the part becomes nonfunctional and the output is stuck at a voltage. When the input stage is damaged, it draws more current or becomes shorted. These two areas are sensitive because they are very difficult to protect without degrading the part's performance. The compensation capacitor has one side tied to a supply pin. This causes it to be directly accessible to the external world. The input cell is designed for a high impedance (large power dissipation) and low capacitance (small in size). Both of these allow an ESD event to cause damage easily. Analog parts as a rule are harder to protect than digital parts. Digital circuits fail with increases in input or output leakage and excess supply current.

ESD failures are caused by at least one of three sources: localized heat generation, high current densities, or high electric field intensities. As discussed earlier, an ESD pulse is modeled as a time varying current source. When the current passes through an IC, an internal current path is established. The conduction processes responsible for this path define the voltage developed and the current densities observed. The product of current density and voltage defines the power density generated. Joule heating causes the local temperature to rise. The thermal mass and thermal resistance in the area of power dissipation define the temperature reached. For protection circuits, it is desired to keep the current density in a circuit element uniform so no point sources of power dissipation occur. Silicon has a negative resistance relationship with temperature, so very high power dissipation in a small volume will result in higher temperatures and thermal runaway. For MOS circuits, the electric field intensity refers to the voltage developed across the dielectric and junctions in the circuit. The gate oxide is the most vulnerable dielectric because it is the thinnest. Structural defects and sharp corners in layouts focus the electric field, making failure more likely at these points.

Each ESD failure mode is traced to one or more of five fundamental damage mechanisms. The mechanisms are listed and summarized in Table 3. A schematic and failure model for each are illustrated in Fig. 18. The most common are oxide rupture and filamentation. Junction spiking is related to filamentation. Thin-film fusing is most common in circuits with thin-film resistors composed of a

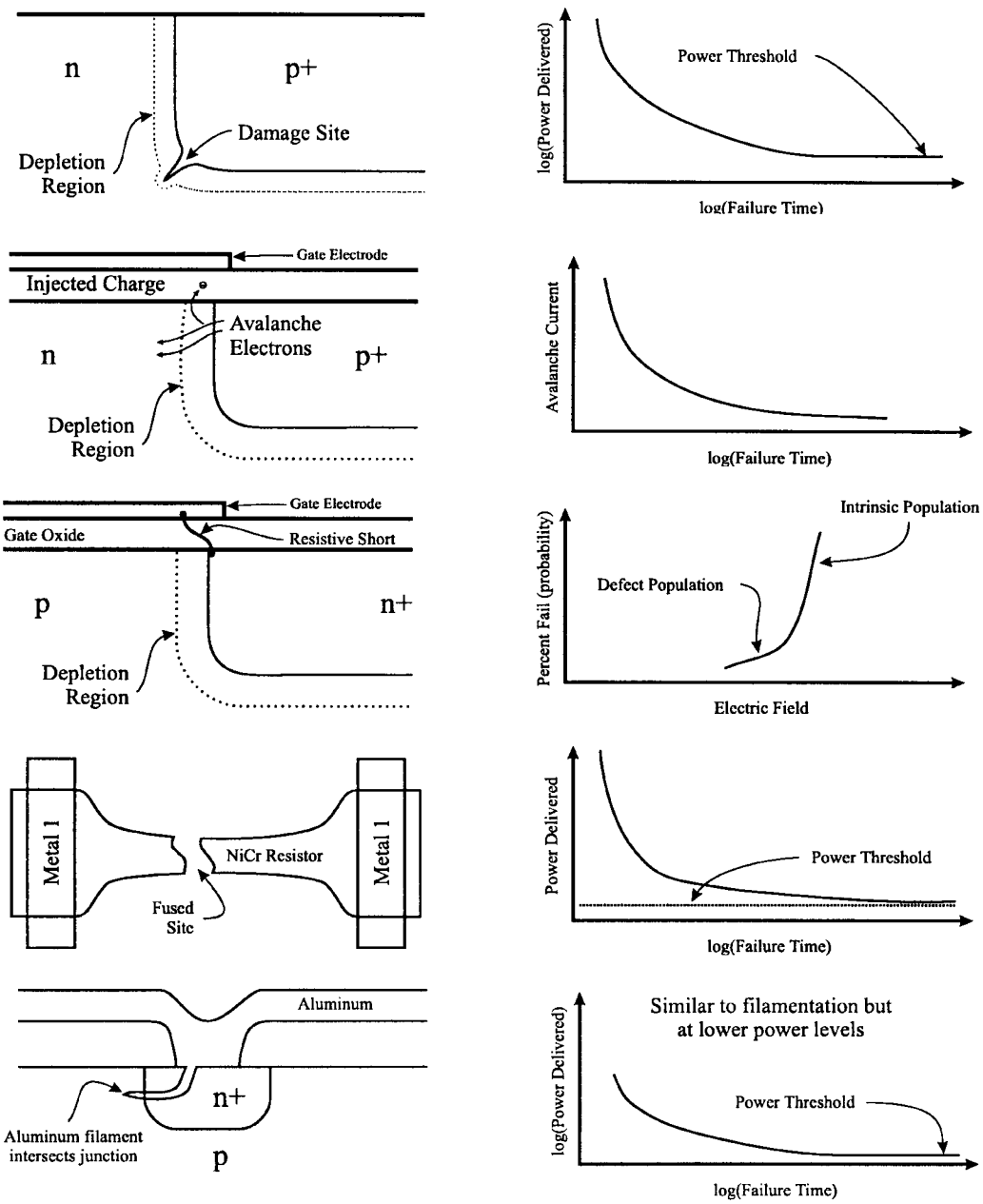

Fig. 18. Damage mechanisms: schematic and failure model.

nickel–chromium (NiCr) alloy. The least common is oxide charging by avalanche injection of carriers into the oxide. In many cases, the charging path results in an oxide rupture rather than just trapped charge in the oxide.

Oxide rupture is dominant in MOS technologies [40]. Here, the induced voltage exceeds the dielectric strength of the oxide, resulting in a rupture. In Fig. 11, the gate oxides of the input transistors are typically those damaged by ESD. The induced voltage caused by the ESD transient is not clamped by the protection circuit to a low enough level to prevent rupture from the gate to the source, body, or drain of the transistor. A small crater is formed under the gate material where a conductive path was established in the dielectric. The gate oxide is not the only concern in integrated circuits. Both bipolar and MOSFET processes can have dielectric ruptures in oxides over active circuitry. This may be the oxide grown over a diffused resistor or an isolation region. If a conductor passes on top of this oxide, a rupture can occur.

Junction filamentation causes an increase in the reverse bias leakage of a p-n junction. In the worst case, the junction is shorted. The ESD event causes current to flow through the junction. The power dissipated in the junction allows the temperature to rise until a region of silicon melts. When silicon melts, its resistance drops by a factor of 30 [14]. This causes more of the current to flow in the melted region, which further heats the melted region, leading to thermal runaway. This phenomenon is referred to as second breakdown [41]. The dopant material redistributes along the melted path. Once the event is over, the power dissipation

stops and the silicon solidifies. The electric field is enhanced at this point, causing increased junction leakage. If the current level is high or if the junction stayed in second breakdown long enough, the site will grow to a shorted junction. In bipolar junction transistors (BJT's) the base-emitter junction is the most susceptible to filamentation damage. Junction spiking is a similar mechanism, except the melted region grows until it intercepts a metal contact, causing an exchange of aluminum and silicon. The damage thresholds are lower for aluminum contacts because the aluminum-silicon eutectic forms at 577°C rather than at the melting point of silicon (1415°C) [33], [42].

Thin-film fusing affects each film in a circuit. These include the metal interconnect, polysilicon interconnect, and thin-film and diffused resistors. The most susceptible to damage are circuits with thin-film resistors. Many precision analog circuits use nickel–chromium (NiCr) alloy resistors as a precision, trimmable resistance element. These resistors are thin ($\sim$200 Å) and have low thresholds for fusing [43]–[49]. The fusing mechanism is described by Davidson *et al.* in [43]. It is important during design that the resistor be made wide enough to handle an ESD current pulse for the desired level of protection. NiCr power densities greater than 3875 W/mm^2 fuse in less than 10 μm with a fusing threshold of 2325 W/mm^2 [43].

The last mechanism is oxide charge injection by avalanche breakdown. This occurs when an ESD event causes a reverse-biased junction to conduct by avalanche multiplication. Some of the carriers have enough energy to surmount the oxide-silicon energy barrier. Electrons are more likely to be injected because the barrier is smaller for them than for holes [51]. If the junction is the drain of a MOSFET, a shift in the threshold voltage results [40]. However, there is a small range where parts are degraded by charge injection but do not result in an oxide rupture [50], [52]. The degree of degradation in oxide reliability is also related to the current density of the injected charge as well as the total charge injected [51], [54]. A localized injection of charge as in a drain avalanche during an ESD transient causes more damage than uniform conduction from the gate to the body of a transistor [54]. Bipolar transistors are also affected by this mechanism. When the junction is the emitter-base of a BJT, the low current h_{fe} shifts. The injected charge distorts the space charge region at the junction surface, increasing the leakage current from base to emitter.

E. Latency

The topic of latent failures as a result of ESD damage has been and continues to be a controversial subject. This subject is discussed between vendor and customer when failures are attributed to ESD. The customer wants assurance that he will not have additional failures if he uses the material. The vendor wants to ship reliable product but has a lot of time and money invested in the material. Both of these desires can be met, as discussed later, but first, an introduction to latency is needed. The term "latency" has come to have several meanings in the context of ESD damage. To help understand latency, it is important to remember that an ESD event is a random occurrence at a fixed point in time. The event is composed of a finite amount of energy delivered to a circuit in a finite amount of time. Once the event is over, that event can no longer cause damage to the circuit. If damage occurs, it does so by a chemical degradation process. The event is outside the normal operating range of the part and as such is a form of electrical overstress. Subsequent ESD events are additional forms of electrical overstress and are not considered in terms of latent damage. The reliability of the part is viewed as the ability of the part to function for a specified amount of time given a set of operating conditions. If the part fails to function under these conditions, it is considered a reliability failure. Failures are caused by chemical mechanisms' leading to a change in the specifications of the device. The leakage current may increase or the part may become nonfunctional. Examples of failure mechanisms are oxide rupture and mobile ionic contamination. These failure sites were manufactured into the part during wafer processing or assembly. If the cause originated at a site generated by ESD damage, then the part would fail because of "latent ESD damage." With this understanding, the following definitions are made.

1) *Latent ESD failure:* a time-dependent failure that is damaged but not detected after an ESD event and results in a permanent detectable failure with subsequent use in normal operation at normal conditions. If the damage is detected prior to use, the part is removed as a reject.
2) *ESD threshold:* the voltage level of an ESD event referenced to a specific ESD discharge model that is capable of producing damage detectable with a specified set of tests.
3) *Testability:* a measure of the ability of a set of electrical tests to detect defects, damage, and changes in operation of a part. This includes any AC (timing measurements), DC (static parameters, i.e., supply current, input leakage, etc.), and functional tests. Data-analysis procedures are also grouped in the testability.

Table 4 provides a summary of 13 papers discussing latency from ESD events. Nine papers say that latency occurs and four say that it does not. Reviewing most of the prolatency papers showed that the type of latency defined is not the same as that defined above. They include a change in the ESD threshold as a sign of latent behavior. McAteer *et al.* [55] supports the fact that if no degradation initially occurs, then the part remains stable throughout its life. In the paper by Gammill and Soden [56], the one failure listed as latent could be a time-dependent dielectric breakdown failure and not latent ESD. A defect in silicon was found at the location. In addition, parts with greater initial shift after ESD testing did not fail. Song *et al.* [54] describe a condition where the reliability of the gate oxide was reduced; however, the units were stressed with a constant

Table 4 Summary of ESD Latency Papers

Ref. #	Device Studied	ESD Technique	Stress Technique	Results
[57, 58, 59]	1409UB 72HC04 Test Chip	HBM, CDM, Charge Pumping	• Single Pulse • Step Stress • Multiple Pulse	Time dependent failures are caused by oxide shorts. Type and location of failure dependent on the type of test performed and the part's past history. Charge trapping observed. Stress hardening observed. Low amplitude pulses produced more latent failures.
[60]	74HCXXX	HBM	• Multiple Pulse • Step Stress	Some stress hardening at high voltages. Poly resistor in protection circuit opened in all failures. Step stress testing showed lower ESD Thresholds than single pulse stressing.
[61]	GaAs MESFETs & Circuits	HBM	• Step Stress • Life Test	No latent damage observed. No stress hardening or weakening of MESFET. No gate oxide in MESFET so not vulnerable to latent defects.
[52]	MOSFET	HBM, Snapback, Charge Pumping	• Multiple Pulse	Trapped charge in oxide that may lead to reduction in immunity to time dependent dielectric breakdown.
[50]	9 different circuits	HBM	• Life Test	No evidence of drift and no failures. DPA on stressed units showed physical damage had occurred but no latency observed in life testing. Damage may effect subsequent ESD susceptibility.
[53]	MOSFET 54L04	HBM	• Life Test	ESD degradation of gate oxide is difficult to achieve and is more prone to catastrophic damage. Trapped charge is typical but anneals at moderate temperatures. ESD degradation of low collector current beta is easier but is stable in life testing.
[55]	Diode, JFET, MOSFET, Logic	HBM	• Life Testing	Devices with no initial degradation after ESD stress remained stable throughout life test. Degraded parts but in specification can worsen.
[56]	CD4035A	HBM	• Life Testing	1 of 40 units failed @ 65 hour in life test. It had < 2% change after zapping. Others with larger shifts did not fail. Pattern defect in silicon at rupture site. Could be TDDB or latency with the authors concluding latency.
[62]	SOS RAM	CDM	• Life Testing	No latency observed but were susceptible to additional ESD events.
[87]	MOS Memory	CDM	• Voltage Ramp • Multiple Pulse	Ramp test on leaky devices showed reduced breakdown voltages. Leakage reduced with time to a minimum value but always greater than virgin transistor.
[54]	MOSFET	Constant Current into drain or gate	• TDDB Testing	All devices showed changes in leakage current. Gate stressed devices showed no significant reduction in life times. Drain stressing reduced life times.

current in the gate or drain but not with an ESD event. No reduction in lifetime was observed in the gate-stressed parts but significant reduction was observed with drain stressing. It is not clear how this constant current stressing simulates a time-dependent voltage and current ESD event.

The evidence is clear that ESD events alter the subsequent ESD threshold of devices either by making them weaker or by stress hardening them [57]–[60]. It is also clear that the major focus by these authors has been the gate oxide as a source of latency. Rubalcava and Roesch [61] conducted a study on GaAs metal–semiconductor (MES)FET devices and circuits. A MESFET has no gate oxide. His study showed no stress hardening and no latent effects. This paper supports the idea that the gate oxide is the cause for changes in ESD threshold.

The remaining papers [50], [53], [62] performed ESD stressing followed by life testing. Many circuits were covered in these experiments. They included discrete transistors, buffers, logic devices, static random-access memory (SRAM), and subscriber-line interface circuits. In all cases, no failures nor evidence of drift occurred. Oren [62] supports the idea of a reduction in the subsequent ESD threshold for devices damaged by ESD. Woodhouse and Lowe [50] took the analysis an extra step and performed a destructive physical analysis on the stressed units after the life test. Each unit showed physical damage, but no latency resulted during the life testing. The damage included dielectric rupture, junction breakdown, and polysilicon resistor damage. Latency as defined here is not probable.

The concern over latency may have originated from low testability of the devices in question. As an example, if an input leakage limit of 100 μA is placed on a pin where the typical leakage is less than 50 nA, then it is easy to allow a damaged pin to escape. It may also be necessary to impose a maximum amount that the pin can change between test points (delta limit). The absolute limit and the delta limit must be chosen based on the device and tester hardware capability. It may be required to create new test techniques like IDDQ (quiescent supply current) testing to increase the testability of a device [63]. This test method looks at each test vector in a quasi-static condition and detects increases in supply current. Defects in the circuit typically manifest

themselves as an increase in supply current, but the defect must be biased to show this extra current. IDDQ testing cycles through a set of test vectors to allow the defects to be biased and detected. To make this test method effective, each stable state in the circuit must have a low current. The design of the circuit can make this a more efficient test by minimizing the use of current sources and free-running oscillators. These devices consume large amounts of current, making the detection limit much higher. This limits its usefulness. If testing considerations are included in the design, it makes detecting and removing defects easier, increasing both the quality and reliability of the product. Selecting the proper test condition can also be an important aspect of increasing the testability of the device. As an example, an SOS SRAM was found to be most sensitive to detecting gate oxide faults at low temperature ($-55°C$). This was caused by a temperature dependent leakage current in SOS material. At room temperature, the leakage component from the SOS material masked any gate oxide defects. By testing at low temperature, the SOS leakage was eliminated and gate defects were observed.

In summary, latency, as defined here, is not likely, provided good test techniques are used. A change in ESD threshold on subsequent events may occur. The apparent ESD threshold is dependent on its past history. The customer/vendor situation discussed at the beginning of this section can be resolved by correcting the cause of the ESD damage. This may involve fixing a ground on the test hardware or better training of the person handling the parts. Once this is accomplished, a rescreen of the devices with tighter leakage and delta limits removes any parts that are damaged but were not detected. The limits should come from a statistical view of each parameter. The outliers are to be removed.

IV. Conclusions

ESD-induced damage is pervasive in semiconductors at both the manufacturer and the end user. The results of ESD damage are costly in physical and people resources as well as time. Because of this, the development of robust circuits and protected environments is required as technology develops. A refocusing of resources at all levels is required to meet the challenges of the future with respect to ESD protection. Advanced protection schemes are necessary and must start with the process architecture used to build integrated circuits. This paper presented a review of ESD and its damage mechanisms with the intent to educate users about ESD and how parts are damaged. It is hoped that this knowledge will aid in the development of fabrication processes and product designs that provide better resistance to these damage mechanisms.

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