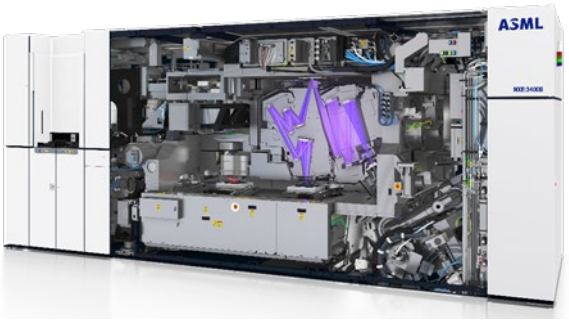
Physics with Industry workshop 2022
Title: Design ASML's next generation tool for 1 nm semiconductor node

1. Company information

ASML is an innovation leader in the semiconductor industry. We provide chipmakers with everything they need – hardware, software and services – to mass produce patterns on silicon through lithography. We enable groundbreaking technology to solve some of society's toughest challenges. Together with our partners, we provide leading patterning solutions that drive the advancement of microchips.
ASML in figures (dec. 2021): 18.6 BEuro turnover; 1984 founded as spin-out from Philips, 32.000 employees (FTE), >10.000 employees in R&D, 120 nationalities

2. Problem

The semiconductor industry is developing at the speed defined by Moore's law. Every two years a new node is introduced enabling faster, cheaper and more energy efficient computing. This is translated into designs of future chips with structures on these chips that get smaller every node. By the end of this decade we will arrive at the 1 nm node.



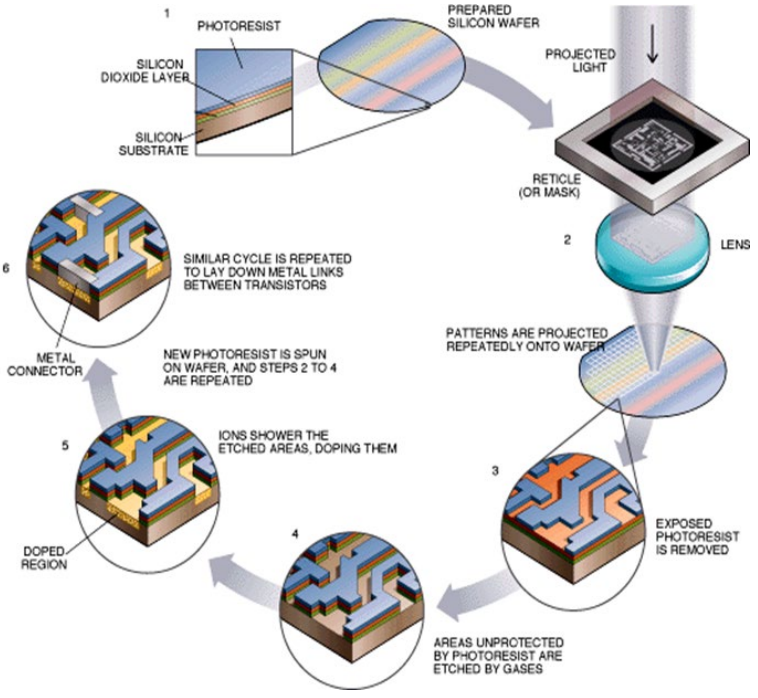
ASML makes machines that our customers use to pattern these small structures on the chip. This is happening at the edges of what physics allows us while it also has to be economically viable. The list of things is very long that we have to control to pattern reliably 200 wafers per hour with 1nm node structures.

Already for decades patterning takes place by exposing a layer of photoresist on the wafer with the image of a mask. After development of the unexposed parts of the photoresist, it acts as a protective layer while the Copper (Cu) structures are etched. The result of all these steps is an interconnect layer in Cu for the billions of transistors in the chip.

For the 1 nm node these Cu interconnects would be that small that their RC-time would limit the speed of the chip. So, we are in need of a material that conducts electrons better than Cu.

Graphene is such a material that has 40% better conductivity than Cu when it is perfect.

Any defect or grain boundary reduces the benefit of graphene. Defects can easily be induced by photoresist application, development or stripping.



So here is the challenge: **develop a patterning technique for structures in graphene that**

- … have conductivity 40% better than Cu
- … have structure size down to 10 nm with <1 nm uniformity
- … can pattern 200 wafers per hour (300 mm)
- … is an extension of Extreme UltraViolet Lithography (EUV)

In literature several solution directions are described. So far, none of them have been able to fulfil all above requirements. Here is a short overview:

Growth of graphene on wafer. For large grain size processing at >400 °C is needed which is not compatible with aprocessed wafer.

Growth and transfer of graphene followed by patterning. Graphene is grown on a dedicated substrate and transferred to the wafer like a blanket. This is not compatible with state-of-art semiconductor manufacturing.

Photoresist patterning. This has good compatibility with existing lithography infrastructure, but shows too many defects.

EUV induced etching. Instead of resist a precursor gas is used that etches graphene under influence of EUV light. Both throughput as well as uniformity of the structures do not meet requirements.

EUV induced deposition. Here a precursor gas is used that locally deposits Carbon that has to be converted into graphene. A dream solution that would also allow deposition of other 2D-materials for transistor channels such as WSe_2 and MoS_2. However, it does not yet meet grain size, throughput, and uniformity.

The scope of this project is limited to

1. Photoresist patterning of graphene with EUV light
2. EUV induced etching
3. EUV induced deposition